ANALYSIS OF FILL FACTOR LOSSES IN THIN FILM CdS/CdTe PHOTOVOLTAIC DEVICES

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Abstract

In this paper, CdS/CdTe solar cells with conversion efficiency values of η = 5.1, 3.6, 3.5, and 2.9% are analyzed and the effects of the device parameters, such as the diode ideality factor (*n*), the saturation current-density (J_o), and the series resistance (R_s,) on the fill factor, both in the dark and under illumination are investigated. The solar cells with efficiency η = 5.1, 3.6, and 2.9% were grown from 3N source material. A solar cell with 3.5% efficiency was made of a 6N CdTe source. The temperature current density-voltage (*J-U-T*) and capacitance-voltage characteristics (*C-U-T*) of CdS/CdTe solar cells were measured in a temperature range of 303-383 K. For all studied cells, the diode ideality factor in the dark is much higher than 2 and the saturation current density increases under illumination, while both the series and shunt resistances decrease under illumination and temperature.

1. Introduction

Thin-film CdS/CdTe devices have been studied extensively, but some basic underlying properties are not well understood, and progress towards higher cell performance has not been rapid. Short circuit current-density (J_{sc}) losses are attributed to reflection, glass absorption, TCO absorption, CdS absorption, and deep-penetration losses. In general, the open circuit voltage (V_{oc}) is limited by the dominant current transport mechanisms. Recombination in the depletion region can reduce the fill factor (*FF*) through the increase in *n*-diode ideality factor and the decrease in V_{oc}. Series resistance (R_s) and shunt resistance (R_{sh}) will also reduce the fill factor, and any voltage dependent current collection, $J_f(U)$, can additionally affect *FF*. To analyze *FF* losses, we used empirical expressions that relate *FF* to the open-circuit voltage V_{oc}, the diode ideality factor *n*, the series resistance R_s, and the shunt resistance R_{sh} [1-3]. In this paper, CdS/CdTe solar cells with conversion efficiency values of η = 5.1, 3.6, 3.5, and 2.9% are analyzed and the effects of the device parameters (n, J_o, R_s,) on the fill factor, both in the dark and under illumination are investigated. An attempt to understand the low fill factor values for these cells is made. The temperature current density-voltage (*J-U-T*) characteristics of CdS/CdTe solar cells are measured in a temperature range of 303-383 K.

2. Experimental

Thin film CdS/CdTe solar cells were grown by close space sublimation [4]. The CdTe thin films were grown from 3N and 6N source material. The CdTe thickness was about 8 μm. CdS thickness was 380 nm. After the CdTe layers were deposited, the structures were held in

$CdCl_2$:H_2O saturated solutions for 3-4 h. After that, the structures were annealed in the air at 390±5°C for 30 min and etched in $K_2Cr_2O_7$:H_2SO_4:H_2O. All cells were completed with a Ni contact thermally deposited in vacuum. SnO_2 served a transparent front contact to CdS. The standard current voltage characteristics were measured at room temperature at 100 mW/cm^2 illumination and in the dark. The light measurements were calibrated to the short circuit current density (J_{sc}) of a Si reference solar cell. At the base of the measure principle of the capacity of the semiconductor junctions, a generator of resonance with circuit LC stands. At the beginning of the experiment, we measured the frequency of the generator without sample that it is studied also without the capacitor of reference. Then, in parallel with the capacitor from circuit LC, the reference calibrated capacitor is connected and the frequency of the generator is measured again. After this, the capacitor of reference is switched off and the studied sample is plugged in. The characteristics of capacitance-voltage are recorded using a program of command and control.

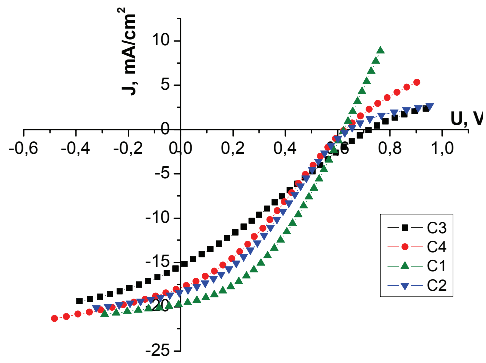

Fig. 1. Current-voltage characteristics of the CdS/CdTe photovoltaic devices under 100 mW/cm^2 illumination: η = (C1) 5.1%, (C2) 3.6%, (C3) 2.9%, and (C4) 3.5%.

3. Analysis and discussion

Figures 1 and 2 illustrate the current-voltage characteristics for a set of the solar cells at the room temperature under illumination of 100 mW/cm^2 through the wide gap component CdS and in the dark, respectively. The devices with η = 5.1, 3.6, and 2.9% denoted as (C1), (C2), and (C3), respectively, were grown from 3N source material and its current-voltage characteristic behaviors in the dark (Fig. 2) are similar. The device with η = 3.5% is denoted as C4 and is grown from a 6N CdTe source. The best photovoltaic parameters are achieved for the C1 device. As one can see from the table, the value of the open circuit voltage (U_{oc}) and current density (J_{sc}) for the C1 device achieves 0.62 V and 19.8 mA/cm^2, respectively.

Photovoltaic parameters of CdS/CdTe photovoltaic devices under 100 mW/cm^2 illumination, T = 300 K.

Cell	**C1**	**C2**	**C4**	**C3**
J_{sc}, mA/cm^2	19.8	18.4	17.8	15.3
U_{oc}, V	0.62	0.64	0.62	0.72
F, %	40	31.0	31.0	26.4
η, %	5.1	3.6	3.5	2.9
R_{sD} Ω·cm^2	123.04	916.648	275.5	1230.4
R_{sL} Ω·cm^2	20.5	28.7	33.5	53.5
R_{sh}D,Ω·cm^2	9.1 10^3	2.5 10^3	5 10^2	6.6 10^3
R_{shL}, Ω·cm^2	157.0	114.57	374.45	93.3
n_D	5.7	3.8	12.8	3.0
n_L	3.0	1.2	5.1	1.6
J_{oD}, mA/cm^2	$5.0\cdot10^{-8}$	$5.2\cdot10^{-8}$	$9.0\cdot10^{-6}$	$1.2\cdot10^{-8}$
J_{oL}, mA/cm^2	2,4E-3	0.5E-6	3.4E-4	2.5E-4

R_{sD}, R_{shD} are the series and shunt resistances in the dark; R_{sI}, R_{shI} are the series and shunt resistances under illumination; n_D is the diode ideality factor in the dark; n_I is the diode ideality factor under illumination. J_{oD} is the saturated current density in the dark; and J_{oL} is the saturated current density under illumination.

Fill factor (*FF)* is low in general. According to the theory, the fill factor is determined by the series resistance, saturated dark current density (J_o), and diode quality factor (n). As one can see from the table, the value of series resistance is high for all devices and is probably due to the fact that the cells used wet $CdCl_2$ treatment that may contain oxide on the surface of CdTe. The fill factor depends on both R_s and R_{sh} in a complex way. As one can see from the table, both R_s and R_{sh} change under illumination. The variation of R_{sh} under illumination is the most dramatic. We may conclude that the light-dependent R_{sh} negatively influences the efficiency of our cells.

The obtaining of high efficiency solar cells requires the understanding of the junction current mechanism transport. Therefore, the temperature current-voltage and capacitance-voltage characteristics of thin film solar cell layers are investigated in a temperature range of 303-383 K. The saturation current J_o and the ideality diode factor are reported, they were obtained by fitting the experimental data to the standard diode equation: $J=J_o \exp(eU/nkT)-1$, where J is the output current density, J_o is the saturation current-density, and n is the diode ideality factor.

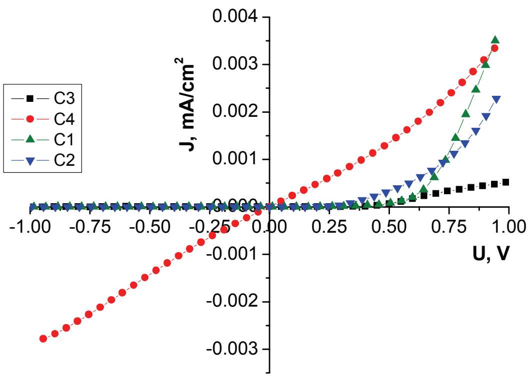

Fig. 2. Dark current-voltage characteristics of the CdS/CdTe solar cells with different efficiencies.

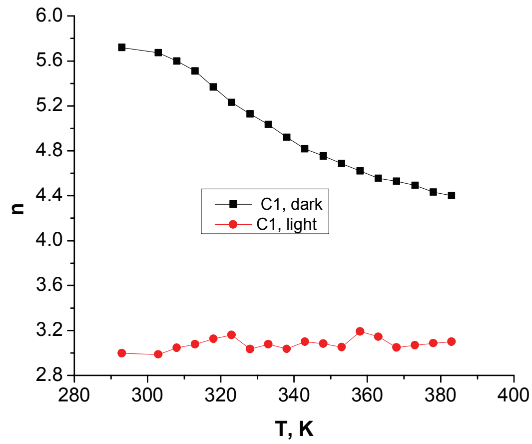

Fig. 3. The ideality factor as a function of temperature; under 100 mW/cm^2 and in the dark for cell C1.

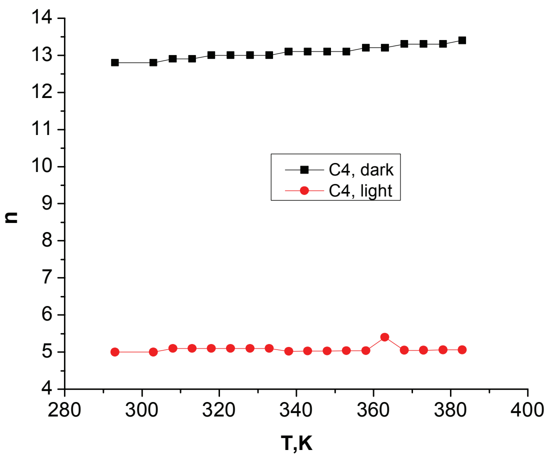

Fig. 4. The ideality factor as a function of temperature; under 100 mW/cm^2 and in the dark for cell C4.

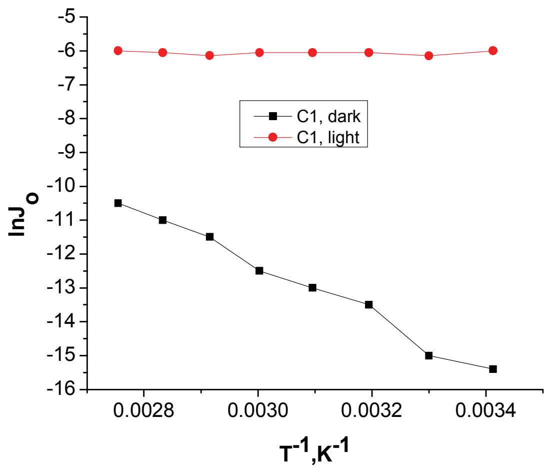

Fig. 5. Plot of ln J_0 vs 1/T for cell C1 under 100 mW/cm2 and in the dark.

For example, photovoltaic device C1 exhibits a temperature-independent n value of ~3 under 100 mW/cm^2 and a temperature-dependent n in the dark (see Fig. 3). Thus, in these cells, generation-recombination current appears to be dominant in the dark. The dominant current flow mechanism under 100 mW/cm^2 illuminations is tunneling.

Photovoltaic device C4 shows a temperature-independent ideality factor value ~13 and higher in the dark and ~5 under 100 mW/cm^2 illumination (see Fig. 4). These data indicate that the tunneling of carriers is an important junction transport mechanism in this cell.

The saturation current-density J_o, which was obtained by extrapolating the forward current curves ln J=$f(U)$ to zero voltage for the C1 device, is found to vary exponentially with $1/T$ in the 300-380 K temperature interval as shown in Fig. 5 according to the relation

$$J_0(T) \approx J_{oo} \exp(-\Delta E_A / kT),$$

where ΔE_A is the activation energy of the charge carriers in the forward bias. The activation energy of the C1 cell calculated from the slope of the ln J_0 vs $1/T$ plot is found to be 0.63 eV close to one-half of the band gap of CdTe. This suggests that the generation-recombination of carriers in the depletion region determines the dark current.

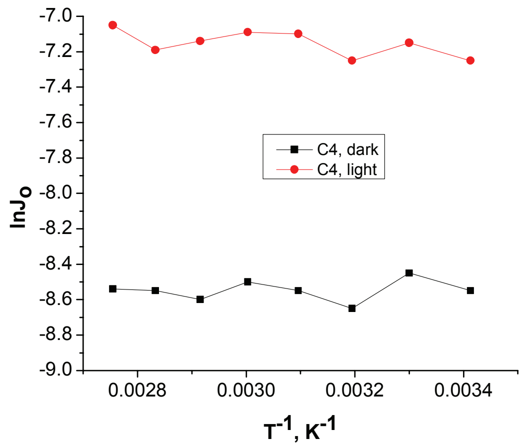

Fig. 6. Plot of ln J_0 vs $1/T$ for cell C4 under 100 mW/cm^2 and in the dark.

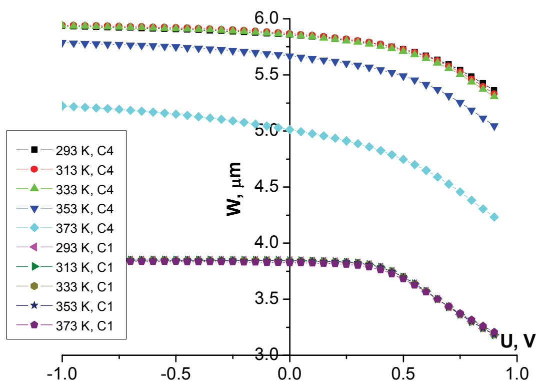

Fig. 7. Depletion layer width (W) as a function of voltage, cells C1 and C4.

It is found that the plot of ln J_0 vs $1/T$ for cell C4 under 100 mW/cm^2 and in the dark does not vary exponentially with reverse temperature interval as shown in Fig. 6.

Capacitance-voltage characteristics at different measurement temperatures for cells C1, C2, and C3 are similar. The curves are almost independent of voltage until forward biases near diffusion potential when the depletion region rapidly collapses leading to an increase in capacitance. Depletion region width versus voltage with temperature variation is not changed for these cells, while for the C4 cell, a decrease in the depletion layer width at higher room temperature is observed (see Fig. 7). This indicates that thermal excitation of carriers between the traps and the energy band in CdTe plays an important role in the behavior of junction in the C4 cell. We observe from Fig. 8 that, for the C1 cell, at all measurement temperatures, the value of the effective carrier concentration in CdTe is close to 10^{17} cm^{-3} near the surface, which is about 3.8 µm away from the CdTe/CdS junction. The value of effective carrier concentration is much lower, ~10^{14} cm^{-3}, in the CdTe region which is 3.0-3.5 µm away from the CdTe/CdS junction. Thus, the CdTe layer appears to be p-type near the surface and p-type (low doped) between the surface and the CdTe/CdS junction. Also, C2 and C3 showed a similar CdTe carrier concentration being relatively high (~10^{17}cm^{-3}) near the surface and low (~10^{14} cm^{-3}) between the surface and the CdTe/CdS junction.

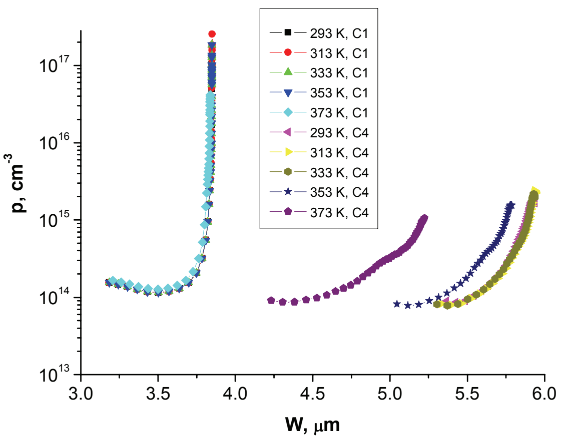

Fig. 8. Dependence of hole density as a function of distance, cells C1 and C4.

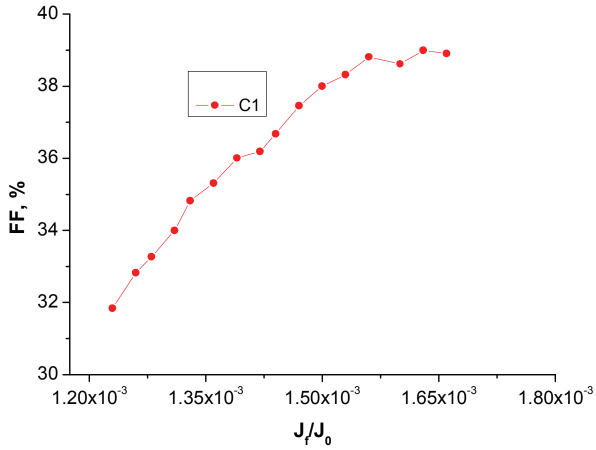

Fig. 9. Variation of fill factor with reverse saturation current, cell C1.

Current-voltage measurements revealed that, under 100 mw/cm^2 illumination, tunneling was the dominant current flow mechanism in these cells and a generation-recombination type current flow process in the dark. Tunneling was also the dominant current flow mechanism in the dark and under illumination for the C4 cell.

The experimental analysis of the fill factor by plotting FF vs J_f/J_o is a useful technique for evaluating the photovoltaic behaviour of solar cells [5]. The curve from Fig. 9 shows the variation of fill factor with reverse saturation current, taking into account the operating current dependence of series resistance (each point is from a *J-U* curve at one illumination) for cell C1. A decrease in FF for high values of J_f/J_o indicates a loss due to series resistance; a decrease in FF for low values of J_f/J_o indicates a parallel resistance loss.

Conclusions

The highest fill factor losses are due to the changes of the saturation current density and ideality factor under temperature and illumination. The FF is a function of series/shunt resistance. Both resistances vary with light level and temperature. The effect of shunt resistance on the fill factor may be neglected in the dark due to high value in all cells. The effect of the series resistance on the fill factor is higher in the dark than under illumination.

Acknowledgements

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